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AMENDMENTS

Please amend the application as indicated hereafter.

To the Specifications:

Please replace paragraph [0017] with the following amended paragraph:

[0017] FIG. 2 is a drawing, ~~schematically~~ showing the typical frequency spectrum of FSK.

Please replace paragraph [0020] with the following amended paragraph:

[0020] FIG. 5 is a process diagram, ~~schematically~~ showing a testing procedure for the FSK modulator, according to one preferred embodiment of this invention.

Please replace paragraph [0029] with the following amended paragraph:

[0029] In the foregoing switching varactor unit 34, it can be designed as the circuit architecture shown in FIG. 4. In FIG. 4, the switching varactor is designed by using bipolar junction diode or metal-oxide semiconductor (MOS) diode. The switching diode unit include a decoder ~~45~~ 46 and a diode pair part. Each diode pair has a diode 34a, and a diode 34b coupled in reverse direction. In other words, the positive ends are commonly coupled to the node X and the other ends of the diodes are coupled to the switching device 42 and 44, respectively. The output end of the switching device 42 is the output terminal VCO_1, and the output end of the switching device 44 is the output terminal VCO_2. The diode pairs are coupled in parallel.

Please replace paragraph [0030] with the following amended paragraph:

[0030] The decoder 46 receives a digital signal with ~~ate~~ at least one bit. In the example, two bits of Mod_1 and Mod_2 are used for descriptions. The decoder 46 has the output channels b0-b3, which have the number equal to 2^n, where n is the input bit number. In the example, n =2. The output channels are respectively coupled to the switching devices 42 and 44 for each diode pairs. The decoder then decodes the quantity of the digital signal and applying the enabling signal to the switching devices, accordingly. For example, when the data 00 is received, then the b0 channel is at enable state, and then the switching devices 42, 44 at the first channel are turned on. Then, the capacitance contributed from the diodes is enabled and added to the VCO core 36 (see FIG. 3). Likewise, if the binary digital data 10 is received, then channels b0 and b2 are turned on. The capacitance from the two channels are added together to have another quantity of capacitance.